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1	(pld fpga field near3 array programmable near4 logic near4 device) and floor$7 and rectangle
2	(pld fpga field near3 array programmable near4 logic near4 device) and floor$7 and rectangle and @ad<"20040329"
3	(pld fpga field near3 array programmable near4 logic near4 device) and floor$7 and rectangle and @ad<"20040329" and "716"/$.ccls.
4	(pld fpga field near3 array programmable near4 logic near4 device) and floor$7 and rectangle and @ad<"20040329" and "716"/$.ccls. and shape same (module block)
5	(pld fpga field near3 array programmable near4 logic near4 device) and floor$7 and @ad<"20040329" and "716"/$.ccls. and shape same (module block cell) and boundar$5 same (module block cell)
6	(pld fpga field near3 array programmable near4 logic near4 device) and floor$7 and @ad<"20040329" and "716"/$.ccls. and shape same (module block cell) and boundar$5 same (module block cell) and (overlap$8 non adj overlap$8 nonoverlap$6)
7	(pld programmable near4 logic near4 decive) same (fpga field near4 array near4 programmable)
8	(pld programmable near4 logic near4 decive) same (fpga field near4 array near4 programmable) and @ad<"20040329"
9	(pld programmable near4 logic near4 decive) same (fpga field near4 array near4 programmable) same (known called) and @ad<"20040329"
10	(pld programmable near4 logic near4 decive) with (fpga field near4 array near4 programmable) with (known called) and @ad<"20040329"
11	(pld programmable near4 logic near4 decive) with (fpga field near4 array near4 programmable) with (known called) and @ad<"20040329" and "716"/$.ccls.
12	(pld fpga programmable near4 (field logic array device)) same (floor$7 partition$4 divi$6) same (module block cell) and (pld fpga programmable near4 (field logic array device)) same (plac$6 same rout$4)
13	(pld fpga programmable near4 (field logic array device)) same (floor$7 partition$4 divi$6) same (module block cell) and (pld fpga programmable near4 (field logic array device)) same (plac$6 same rout$4) and @ad<"20040329" and "716"/$.ccls.
14	(pld fpga programmable near4 (field logic array device)) same (floor$7 partition$4 divi$6) same (module block cell) and (pld fpga programmable near4 (field logic array device)) same (plac$6 same rout$4) and @ad<"20040329" and "716"/$.ccls. and (module block cell) same (boundar$4 ovelap$6)
15	(pld fpga programmable near4 (field logic array device)) same (floor$7 partition$4 divi$6) same (module block cell) and (pld fpga programmable near4 (field logic array device)) same (plac$6 same rout$4) and @ad<"20040329" and "716"/$.ccls. and (module block cell) same (boundar$4 border ovelap$6)
16	(pld fpga programmable near4 (field logic array device)) same (floor$7 partition$4 divi$6) same (module block cell) and (pld fpga programmable near4 (field logic array device)) same (plac$6 same rout$4) and @ad<"20040329" and "716"/$.ccls. and (module block cell) same (boundar$4 border ovelap$6) and (module block cell) with (shape siz$4 dimension)
17	(pld fpga programmable near4 (field logic array device)) same (floor$7 plac$6 partition$4 divi$6) same (module block cell) and (pld fpga programmable near4 (field logic array device)) same (plac$6 same rout$4) and @ad<"20040329" and "716"/$.ccls. and (module block cell) same (boundar$4 border ovelap$6) and (module block cell) with (shape siz$4 dimension)

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18	(pld fpga programmable near4 (field logic array device)) same (floor$7 plac$6 partition$4 divi$6) same (module block cell) and (pld fpga programmable near4 (field logic array device)) same (plac$6 same rout$4) and @ad<"20040329" and "716"/$.ccls. and (module block cell) same (boundar$4 border ovelap$6) and (module block cell) with (shape siz$4 geometry dimension)
19	"6490717".pn. and (pld fpga programmable near4 (field logic array device)) and (cell block module)
20	"6490717".pn. and (pld fpga programmable near4 (field logic array device)) and (cell block module)
21	"5483461".pn.
22	"20020166098" ("5808330" "5930499" "5953236" "6766500" "6817005" "5822214" "5818729" "5778216" "6002857" "6301693").pn.
23	"20020166098" ("5808330" "5930499" "5953236" "6766500" "6817005" "5822214" "5818729" "5778216" "6002857" "6301693").pn.
24	"6490717".pn.
25	"20020166098" ("5808330" "5930499" "5953236" "6766500" "6817005" "5818729" "5778216" "6002857").pn.
26	"20020166098" ("5808330" "5930499" "5953236" "6766500" "6817005" "5818729" "5778216" "6002857" "5483461" "6134702" "5309371").pn.
27	"20020166098" ("5808330" "5930499" "5953236" "6766500" "6817005" "5822214" "5818729" "5778216" "6002857" "6301693" "5483461" "6134702" "5309371").pn.
28	"20020166098" ("5808330" "5930499" "5953236" "6766500" "6817005" "5822214" "5818729" "5778216" "6002857" "6301693" "5483461" "6134702" "5309371").pn. and (pld fpga)
29	"20020166098" ("5808330" "5930499" "5953236" "6766500" "6817005" "5822214" "5818729" "5778216" "6002857" "6301693" "5483461" "6134702" "5309371").pn. and (pld fpga) and plac$5 same rout$5
30	("20020166098" ("5808330" "5930499" "5953236" "6766500" "6817005" "5822214" "5818729" "5778216" "6002857" "6301693" "5483461" "6134702" "5309371").pn.) and (pld fpga) and plac$5 same rout$5
31	("20020166098" ("5808330" "5930499" "5953236" "6766500" "6817005" "5822214" "5818729" "5778216" "6002857" "6301693" "5483461" "6134702" "5309371").pn.) and (pld fpga) and plac$5 same rout$5 and (ovelap$5 boundar$4) same (cell block module)
32	(pld fpga programmable near4 (field logic array device)) and (floor$7 partition$4 divi$6) same (module block cell) and (pld fpga programmable near4 (field logic array device)) same (plac$6 same rout$4) and @ad<"20040329" and "716"/$.ccls. and (module block cell) same (boundar$4 border$4 ovelap$6)
33	(pld fpga programmable near4 (field logic array device)) and (floor$7 partition$4 divi$6) same (module block cell) and (pld fpga programmable near4 (field logic array device)) same (plac$6 same rout$4) and @ad<"20040329" and "716"/$.ccls. and (module block cell) same (boundar$4 border$4 ovelap$6) and (module block cell) with (siz$4 shap$4 dimension$4 geometry width height)
34	"5818729".pn.
35	"5818729".pn. and (pld fpga)
36	"20050086624" and (pld fpga)

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37	"20050086624" "."
38	(pld fpga programmable near4 (field logic array device)) and (adjust$4 modif$6) same (module block cell) same (boundar$4 shape siz$4 dimension) and (pld fpga programmable near4 (field logic array device)) same (plac$6 same rout$4) and @ad<"20040329" and (module block cell) same (boundar$4 border ovelap$6) and (module block cell) with (shape siz$4 dimension)

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1	(pld fpga) and floor$8 same (alter$6 chang$4 modif$7)
2	(module block cell) same (chang$7 alter$7 modif$7)
3	((pld fpga) and floor$8 same (alter$6 chang$4 modif$7)) and ((module block cell) same (chang$7 alter$7 modif$7)) and "716"/$.ccls.
4	((pld fpga) and floor$8 same (alter$6 chang$4 modif$7)) and ((module block cell) same (chang$7 alter$7 modif$7)) and "716"/$.ccls. and @ad<"20020329"
5	(((pld fpga) and floor$8 same (alter$6 chang$4 modif$7)) and ((module block cell) same (chang$7 alter$7 modif$7)) and "716"/$.ccls. and @ad<"20020329") and (fpga field near5 gate near5 programmable)
6	((((pld fpga) and floor$8 same (alter$6 chang$4 modif$7)) and ((module block cell) same (chang$7 alter$7 modif$7)) and "716"/$.ccls. and @ad<"20020329") and (fpga field near5 gate near5 programmable)) and (percen$6) same (chang$7 alter$7 modif$7)
7	((((pld fpga) and floor$8 same (alter$6 chang$4 modif$7)) and ((module block cell) same (chang$7 alter$7 modif$7)) and "716"/$.ccls. and @ad<"20020329") and (fpga field near5 gate near5 programmable)) and (percen$6)
8	(module block cell) same (chang$7 alter$7 modif$7)
9	(module block cell) with (chang$7 alter$7 modif$7)
10	(pld fpga) and floor$8 with (alter$6 chang$4 modif$7)
11	((pld fpga) and floor$8 with (alter$6 chang$4 modif$7)) and (module block cell) same (chang$7 alter$7 modif$7)
12	(((pld fpga) and floor$8 with (alter$6 chang$4 modif$7)) and (module block cell) same (chang$7 alter$7 modif$7)) and "716"/$.ccls.
13	(pld fpga) and floor$8 with (alter$6 chang$4 modif$7)
14	((pld fpga) and floor$8 with (alter$6 chang$4 modif$7)) and (module block cell) with (chang$7 alter$7 modif$7)
15	(((pld fpga) and floor$8 with (alter$6 chang$4 modif$7)) and (module block cell) with (chang$7 alter$7 modif$7)) and "716"/$.ccls.
16	((((pld fpga) and floor$8 with (alter$6 chang$4 modif$7)) and (module block cell) with (chang$7 alter$7 modif$7)) and "716"/$.ccls.) and @ad<"20020329"
17	(((((pld fpga) and floor$8 with (alter$6 chang$4 modif$7)) and (module block cell) with (chang$7 alter$7 modif$7)) and "716"/$.ccls.) and @ad<"20020329") and (fpga field near5 gate near5 programmable)
18	((((((pld fpga) and floor$8 with (alter$6 chang$4 modif$7)) and (module block cell) with (chang$7 alter$7 modif$7)) and "716"/$.ccls.) and @ad<"20020329") and (fpga field near5 gate near5 programmable)) and plac$4 same rout$4
19	(((((((pld fpga) and floor$8 with (alter$6 chang$4 modif$7)) and (module block cell) with (chang$7 alter$7 modif$7)) and "716"/$.ccls.) and @ad<"20020329") and (fpga field near5 gate near5 programmable)) and plac$4 same rout$4) and percent$5

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20	(((((((pld fpga) and floor$8 with (alter$6 chang$4 modif$7)) and (module block cell) with (chang$7 alter$7 modif$7)) and "716"/$.ccls.) and @ad<"20020329") and (fpga field near5 gate near5 programmable)) and plac$4 same rout$4) and percent$5 same (alter$6 chang$4 modif$7)
21	(((((((pld fpga) and floor$8 with (alter$6 chang$4 modif$7)) and (module block cell) with (chang$7 alter$7 modif$7)) and "716"/$.ccls.) and @ad<"20020329") and (fpga field near5 gate near5 programmable)) and plac$4 same rout$4) and non-overlap$7
22	(((((((pld fpga) and floor$8 with (alter$6 chang$4 modif$7)) and (module block cell) with (chang$7 alter$7 modif$7)) and "716"/$.ccls.) and @ad<"20020329") and (fpga field near5 gate near5 programmable)) and plac$4 same rout$4) and overlap$7
23	(((((((pld fpga) and floor$8 with (alter$6 chang$4 modif$7)) and (module block cell) with (chang$7 alter$7 modif$7)) and "716"/$.ccls.) and @ad<"20020329") and (fpga field near5 gate near5 programmable)) and plac$4 same rout$4) and (module block cell) same (chang$7 alter$7 modif$7) same (siz$4 shap$5 dimension)
24	(pld fpga) and floor$8 and plac$7 with rout$7 and (alter$6 chang$4 modif$7 adjust$7 generat$5) same (cell module block) same (dimension size shape width length height high wide)
25	S24 and (overlap$6 non adj overlap$7)
26	S24 and (overlap$6 non adj overlap$7) and @ad<"20040329"
27	S26 and (fpga field with programmable with gate) and "716"/$.ccls.
28	S26 and (fpga field with programmable with gate) and "716"/$.ccls. and boundar$4
29	("20010047509" "5822214".pn.) and percent$4
30	("20010047509" "5822214".pn.) and increment$5 same (chang$4 alter$7 modi$6 adjust$6)
31	("20010047509" "5822214".pn.) and (chang$4 alter$7 modi$6 adjust$6 increas$4 decreas$4) same (component cell module block)
32	(chang$4 alter$7 modi$6 adjust$6 increas$4 decreas$4) same (component cell module block) same percent$4
33	(chang$4 alter$7 modi$6 adjust$6 increas$4 decreas$4) same (component cell module block) same percent$4 and @ad<"20040329"
34	(chang$4 alter$7 modi$6 adjust$6 increas$4 decreas$4) same (component cell module block) same percent$4 and @ad<"20040329" and floorplan$4
35	(chang$4 alter$7 modi$6 adjust$6 increas$4 decreas$4) same (component cell module block) same percent$4 and @ad<"20040329" and floorplan$4 and (pld fpga programmable)
36	(pld fpga) same floor$8 same (alter$6 arrang$4 allocat$4 partition$6 chang$4 modif$7)
37	(pld fpga) same floor$8 same (alter$6 arrang$4 allocat$4 partition$6 chang$4 modif$7) and @ad<"20040329"

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38	(pld fpga) same floor$8 same (alter$6 arrang$4 allocat$4 partition$6 chang$4 modif$7) and @ad<"20040329" and "716"/$.ccls. and (chang$6 adjust$6 modif$6 alter$7) same (siz$4 shap$4 dimesion$4 height length)
39	(pld fpga) same floor$8 same (alter$6 arrang$4 allocat$4 partition$6 chang$4 modif$7) and @ad<"20040329" and "716"/$.ccls. and (chang$6 adjust$6 modif$6 alter$7 generat$4 creat$4) same (siz$4 shap$4 dimesion$4 height length width) same (block module)
40	"5822214".pn.
41	"20050023947"
42	"20050023947" and ("120" tube arc lamp double spiral dischar$5)
43	(pld fpga) same floor$8 same (alter$6 arrang$4 allocat$4 partition$6 chang$4 modif$7) and @ad<"20040329" and "716"/$.ccls.